

CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:
 - 2 a microprocessor coupled to a primary bridge device;
 - 3 a main memory array coupled to a memory controller by way of a memory bus, said
 - 4 memory controller integral with said primary bridge device;
 - 5 a secondary bridge device coupled to said primary bridge device by way of a primary
 - 6 expansion bus;
 - 7 an input/output controller coupled to said secondary bridge device by way of a secondary
 - 8 expansion bus;
 - 9 a read only memory (ROM) coupled to said secondary bridge device by way of the
 - 10 secondary expansion bus, said ROM stores programs executable by the microprocessor;
 - 11 a keyboard coupled to said input/output controller;
 - 12 a host clock generator having a host clock signal coupled to a phase locked loop (PLL)
 - 13 device and said memory controller;
 - 14 said PLL device having a plurality of PLL output signals having the same frequency as the
 - 15 host clock output signal, but differing in phase relationship;
 - 16 one of said PLL outputs signals coupled to said main memory array, and one of said PLL
 - 17 output signals coupled to said memory controller;
 - 18 a clock delay circuit coupled between said PLL output signal and said memory controller,
 - 19 said clock delay circuit time delays said PLL output signal, said clock delay circuit comprising:
 - 20 a first signal path having a first length, said first signal path selectable by a first
 - 21 electrically controlled switch coupled to the first signal path; and

22 a second signal path having a length longer than said first length, said second signal
23 path selectable by a second electrically controlled switch coupled to the second signal path;
24 wherein said clock delay circuit routes said PLL output signal along one of said first signal
25 path for a short time delay, and said second signal path for a long time delay.

1 2. The computer system as defined in claim 1 wherein said electrically controlled switches
2 further comprise field effect transistors (FETs), thereby creating a first and second FET coupled to
3 the first and second signal paths respectively.

1 3. The computer system as defined in claim 2 further comprising:
2 a gate of said first FET coupled to an output signal of a control device;
3 a gate of said second FET coupled to an output signal of the control device;
4 the output signals of said control device are selectively asserted and de-asserted by
5 command of software instructions stored on said ROM device and executed by said
6 microprocessor; and
7 wherein the assertion and de-assertion of the output signals acts to select one of the first
8 and second signal paths.

1 4. The computer system as defined in claim 3 wherein the control device further comprising
2 said secondary bridge device.

1 5. The computer system as defined in claim 3 wherein the control device further comprising
2 said input/output controller.

1 6. The computer system as defined in claim 3 wherein said software instructions stored on
2 said ROM determines a number of dual inline memory modules (DIMMs) present in the main
3 memory array of said computer system, and configures the time delay implemented by the clock
4 delay circuit based on the number of DIMMs by asserting and de-asserting outputs of said control
5 device.

1 7. The computer system as defined in claim 6 wherein said software instructions on said
2 ROM device further comprises a look-up table that indicates the selection of one of the first and
3 second signal paths as a function of the number of DIMMs present in the main memory array of
4 the computer system.

1 8. The computer system as defined in claim 6 wherein said software instructions on said
2 ROM tests each path of the first and second signal of said clock delay circuit to determine a
3 shortest possible path length to implement as a function of which path length is the shortest useable
4 length without invoking bit errors in data transfers.

1 9. The computer system as defined in claim 6 wherein said control device is the secondary
2 bridge device.

1 10. The computer system as defined in claim 3 wherein said output signals of said control
2 device further comprise digital output signals.

1 11. The computer system as defined in claim 1 further comprising:
2 a phase lag circuit coupled within a feedback path of the PLL device adjusts the phase of
3 the PLL output signals in relation to the host clock signal by selectively implementing different
4 lengths of the feedback path by the selective assertion of one of a plurality of electrically controlled
5 switches, said switches coupled one each to a plurality of feedback signal paths of varying lengths.

1 12. The computer system a defined in claim 11 wherein said plurality of feedback signal paths
2 of varying lengths further comprise:

3 a first feedback signal path having a length coupled to and selectable by a first feedback
4 FET; and
5 a second feedback signal path having a length longer than said first feedback signal path,
said second feedback signal path coupled to and selectable by a second feedback FET.

1 13. The computer system as defined in claim 12 further comprising:

2 a gate of said first feedback FET coupled to an output signal of a control device;
3 a gate of said second feedback FET coupled to an output signal of the control device; and
4 wherein said ROM device stores software instructions, executed by said microprocessor,
5 which selectively assert one of the output signals of the control device to implement the feedback
6 path with a length that includes one of said first and second signal paths.

1 14. The computer system as defined in claim 13 wherein said selective assertion of output
2 signals by the software instructions is based on a required phase lag between the host clock signal
3 and the PLL output signals as a function of parasitic capacitance present on the memory bus.

1 15. The computer system as defined in claim 13 wherein said control device further comprises
2 the secondary bridge device.

1 16. The computer system as defined in claim 13 wherein said control device further comprises
2 the input/output controller.

1 17. A method of adaptively compensating for parasitic capacitance on a bus transferring data
2 from a sending device to a receiving device, comprising:

3 coupling a plurality of signal paths, at least two of the plurality having different path
4 lengths, between a source of a read clock and the receiving device, which receiving device uses the
5 read clock as a trigger to read data from the bus;

6 selecting one of the signal paths, based at least in part on the parasitic capacitance, by
7 forcing an electrically controlled switch into a conduction mode, for the path desired, and by
8 forcing remaining electrically controlled switches, associated with other paths, into a non-
9 conductive mode; thereby

10 adjusting a phase relationship between the read clock and a write clock, used by the
11 sending device as a trigger to drive data to the bus.

1 18. The method as defined in claim 17 wherein forcing the electrically controlled switches into
2 conductive and nonconductive modes further comprises:

3 asserting a first output signal of a control device coupled to a gate connection of a first
4 FET, and substantially simultaneously deasserting a second output signals of the control device
5 coupled to a gate connection of a second FET; thereby

6 passing the read clock through the first FET and one of said plurality of signal paths; and
7 preventing the passage of the read clock through the second FET, thereby disallowing
8 propagation of said read clock through remaining signal paths of the plurality of signal paths.

1 19. The method as defined in claim 18 wherein selecting one of the signal paths further
2 comprises:

3 determining a number of dual inline memory modules (DIMMs) present in said sending
4 device; and

5 referring to a look-up table which directs the use of one of said signal path based on the
6 number of DIMMs present.

1 20. The method as defined in claim 18 wherein selecting one of the signal paths further
2 comprises determining a shortest signal path length of the read clock at which data transfers
3 between the sending device and the receiving device occur without error.

1 21. The method as defined in claim 20 wherein determining the shortest signal path length
2 further comprises:

3 testing each signal path from a longest path length to the shortest path length by
4 transferring test data from the sending device to the receiving device and checking for bit errors,

5 said testing continued until the signal path length used for the read clock causes bit errors in the
6 transfer of the test data; and

7 selecting a path length for the read clock at which no bit errors occurred in the transfer of
8 test data.

1 22. A system to control phase lag of clock signals within a computer system, comprising:
2 a host clock device having a host clock (HCLK) output signal;
3 said HCLK output signal coupled to an input signal of a phase locked loop (PLL) device
4 and an input signal of a memory controller;

5 a main memory array coupled to said memory controller by way of a memory bus, said
6 memory array comprising at least one dual inline memory module (DIMM), said DIMM coupled
7 to and adding a parasitic capacitance to the memory bus;

8 a PLL output clock signal coupled to said memory controller, said memory controller
9 adapted to read data on said memory bus responsive to said PLL output clock signal;

10 a read clock (RDCLK) delay circuit coupled between the PLL output clock signal and the
11 memory controller;

12 at least one control signal coupled to said RDCLK delay circuit; and

13 wherein the RDCLK delay circuit selectively implements varying length paths for the
14 RDCLK signal responsive to the control signal.

1 23. The system to control phase lag of clock signals within a computer system as defined in
2 claim 22 wherein said RDCLK delay circuit further comprises:

3 a first signal path having a first length, said first signal path selectable by a first electrically
4 controlled switch coupled to the first signal path;
5 a second signal path having a length longer than said first length, said second signal path
6 selectable by a second electrically controlled switch coupled to the second signal path;
7 each of said electrically controlled switches having a control input connection coupled to
8 the control signal; and
9 wherein said clock delay circuit routes the PLL output signal along one of said first signal
10 path for a short phase delay, and said second signal path for a long phase delay.

1 24. The system to control phase lag of clock signals in a computer system as defined in
2 claim 23 wherein the electrically controlled switches of said RDCLK delay circuit further
3 comprise:

4 field effect transistors (FETs), each having a gate connection; and
5 the control signal coupled to the gate of each FET.

1 25. The system to control phase lag of clock signals in a computer system as defined in
2 claim 24 further comprising:
3 an output signal of a bridge device coupled to the at least one control signal;
4 a software program executed by a microprocessor selectively asserting the output signal of
5 the bridge device based, at least in part, on a number of DIMMs present in said computer system.

1 26. The system to control phase lag of clock signals in a computer system as defined in
2 claim 23 further comprising:

3 a first FET having its drain coupled to a first end of the first signal path, and a second FET

4 having its source coupled to a second end of the first signal path;

5 a third FET having its drain coupled to a first end of the second signal path, and a fourth

6 FET having its source coupled to a second end of the second signal path;

7 gate connections of the first and second FETs coupled to each other, and further coupled to

8 the at least one control signal;

9 gate connections of the third and fourth FETs coupled to each other, and further coupled to

10 the at least one control signal; and

11 the RDCLK delay circuit implements the first signal path when said first and second FETs

12 are in a conductive mode responsive to the at least one control signal, and said RDCLK delay

13 circuit further implements the second signal path when said third and fourth FETs are in a

14 conductive mode responsive to their gates signal.

1 27. The system to control phase lag of clock signals in a computer system as defined in

2 claim 23 further comprising:

3 the gate connections of the first and second FETs coupled to a first control signal;

4 the gate connections of the third and fourth FETs coupled a second control signal;

5 each of said first and second control signals coupled to output signals of a control device;

6 and

7 wherein said output signals of the control device are selectively asserted and de-asserted by

8 a software program, executed by a microprocessor.

1 28. The system to control phase lag of clock signals in a computer system as defined in
2 claim 27 further comprising:

3 the control device is a secondary bridge device; and
4 the software program is stored on a read only memory coupled to said secondary bridge
5 device.

1 29. The system to control phase lag of clock signals in a computer system as defined in
2 claim 22 further comprising:

3 said PLL device having a feedback path, the length of said feedback path controls the phase
4 relationship between the input signal of the PLL device and PLL output signals; and
5 a feedback delay circuit coupled within the feedback path of the PLL device, said feedback
6 delay circuit adapted to selectively change the length of said feedback path, said feedback delay
7 circuit comprising:

8 a first feedback path having a length, said first feedback path selectable by a first
9 electrically controlled switch coupled to the first feedback path; and

10 a second feedback path having a length longer than the length of the first feedback
11 path, said second feedback path selectable by a second electrically controlled switch coupled to the
12 second feedback path.

1 30. A method of adaptively controlling phase shift of clock signals in a computer system,
2 comprising:

3 coupling a host clock signal to a phase locked loop (PLL) device, and a memory controller;
4 coupling the memory controller to a main memory array;

5 coupling a first PLL output signal to a variable length clock path circuit;
6 coupling a variable length clock path circuit output signal to the memory controller;
7 adjusting a length of a clock path through said variable length clock path circuit so as to
8 selectively time delay the variable length clock path output signal relative to the first PLL output
9 signal, wherein said adjusting further comprises:
10 activating a first electrically controlled switch to select a first clock path having a
11 desired length; and
12 refraining from activating a second electrically controlled switch and thereby not
13 selecting a second clock path.

1 31. The method as defined in claim 30 further comprising:
2 implementing a variable length feedback path circuit in a feedback path of the PLL device;
3 determining the number of dual inline memory modules (DIMMs) present in a main
4 memory array;
5 adjusting the length of the feedback path of the PLL device as a function of the number of
6 DIMMs to adjust the phase relationship between the host clock signal and PLL output signals, said
7 adjusting accomplished by selecting one of a plurality of possible path lengths in the variable
8 length feedback path circuit by actuating an electrically controlled switch.

1 32. A system to control phase lag of clock signals within a computer system, comprising:
2 a host clock device having a host clock (HCLK) output signal;
3 said HCLK output signal coupled to an input signal of a phase locked loop (PLL) device
4 and an input signal of a memory controller;

5 a main memory array coupled to said memory controller by way of a memory bus, said
6 memory array comprising at least one dual inline memory module (DIMM), said DIMM coupled
7 to and adding a parasitic capacitance to the memory bus;
8 a PLL output clock signal coupled to said memory controller, said memory controller
9 adapted to read data on said memory bus responsive to said PLL output clock signal;
10 said PLL device having a feedback path, the length of said feedback path controls the phase
11 relationship between the input signal of the PLL device and PLL output signals;
12 a feedback delay circuit coupled within the feedback path of the PLL device;
13 at least one control signal coupled to said feedback delay circuit;
14 said feedback delay circuit selectively changes the length of said feedback path responsive
15 to the control signal.

1 33. The system to control phase lag of clock signals within a computer system as defined in
2 claim 32 wherein said feedback delay circuit further comprises:
3 a first signal path having a first length, said first signal path selectable by a first electrically
4 controlled switch coupled to the first signal path;
5 a second signal path having a length longer than said first length, said second signal path
6 selectable by a second electrically controlled switch coupled to the second signal path;
7 each of said electrically controlled switches having a control input connection coupled to
8 the control signal; and
9 wherein said feedback delay circuit routes the PLL feedback path along one of said first
10 signal path for a short phase delay, and said second signal path for a long phase delay.

1 34. The system to control phase lag of clock signals in a computer system as defined in
2 claim 33 wherein the electrically controlled switches of said feedback delay circuit further
3 comprise:

4 field effect transistors (FETs), each having a gate connection; and
5 the control signal coupled to the gate of each FET.

1 35. The system to control phase lag of clock signals in a computer system as defined in
2 claim 34 further comprising:

3 an output signal of a bridge device coupled to the at least one control signal;
4 a software program executed by a microprocessor selectively asserting the output signal of
5 the bridge device based, at least in part, on a number of DIMMs present in said computer system.

1 36. The system to control phase lag of clock signals in a computer system as defined in
2 claim 33 further comprising:

3 a first FET having its drain coupled to a first end of the first signal path, and a second FET
4 having its source coupled to a second end of the first signal path;

5 a third FET having its drain coupled to a first end of the second signal path, and a fourth
6 FET having its source coupled to a second end of the second signal path;

7 gate connections of the first and second FETs coupled to each other, and further coupled to
8 the at least one control signal;

9 gate connections of the third and fourth FETs coupled to each other, and further coupled to
10 the at least one control signal; and

11 the feedback delay circuit implements the first signal path when said first and second FETs
12 are in a conductive mode responsive to the at least one control signal, and said feedback delay
13 circuit further implements the second signal path when said third and fourth FETs are in a
14 conductive mode responsive to their gates signal.

1 37. The system to control phase lag of clock signals in a computer system as defined in
2 claim 36 further comprising:

3 the gate connections of the first and second FETs coupled to a first control signal;
4 the gate connections of the third and fourth FETs coupled a second control signal;
5 each of said first and second control signals coupled to output signals of a control device;
6 and

7 wherein said output signals of the control device are selectively asserted and de-asserted by
8 a software program, executed by a microprocessor.

1 38. The system to control phase lag of clock signals in a computer system as defined in
2 claim 37 further comprising:

3 the control device is a secondary bridge device; and
4 the software program is stored on a read only memory coupled to said secondary bridge
5 device.

1 39. The system to control phase lag of clock signals in a computer system as defined in
2 claim 32 further comprising:

3 a read clock (RDCLK) delay circuit coupled between the PLL output clock signal and the

4 memory controller;

5 at least one control signal coupled to said RDCLK delay circuit; and

6 wherein the RDCLK delay circuit selectively implements varying length paths for the

7 RDCLK signal responsive to the control signal, said RDCLK delay circuit comprising:

8 a first clock path having a length, said first clock path selectable by a first

9 electrically controlled switch coupled to the first clock path; and

10 a second clock path having a length longer than the length of the first clock path,

11 said second clock path selectable by a second electrically controlled switch coupled to the second

12 clock path.